CLAIMS

What is claimed is:

1. A programmable logic device (PLD), comprising:

a system clock input pad providing a system clock input signal;

a system clock buffer having an input terminal coupled to the system clock input pad and further having an output terminal;

a central node coupled to the output terminal of the system clock buffer;

a plurality of secondary clock buffers each having an input terminal coupled to the central node and each further having an output terminal;

a plurality of programmable logic blocks divided into sets, each set including a plurality of programmable logic blocks, each set having an associated secondary clock buffer, each programmable logic block having an input clock terminal; and

a plurality of synthesizer circuits, each synthesizer circuit having an associated programmable logic block, each synthesizer circuit being coupled between the input clock terminal of the associated programmable logic block and the output terminal of the associated secondary clock buffer,

wherein each synthesizer circuit comprises means for selectively decoupling the input clock terminal of the associated programmable logic block from the output terminal of the associated secondary clock buffer and providing a steady-state signal to the input clock terminal of the associated programmable logic block.

2. The PLD of Claim 1, wherein the steady-state signal is a ground signal.

3. The PLD of Claim 1, wherein the steady-state signal is a power high signal.

4. The PLD of Claim 1, wherein at least one of the system clock buffer and the secondary clock buffers are inverting buffers.

5. The PLD of Claim 1, wherein the central node is located about at the center of the PLD.

6. The PLD of Claim 1, wherein each synthesizer circuit further comprises:

means for selectively deriving an output clock signal from an input clock signal on the output terminal of the associated secondary clock buffer and providing the output clock signal to the input clock terminal of the associated programmable logic block.

7. The PLD of Claim 6, wherein the output clock signal has a rising edge corresponding to a rising edge of the input clock signal.

8. The PLD of Claim 6, wherein the output clock signal has a rising edge corresponding to a falling edge of the input clock signal.

9. The PLD of Claim 6, wherein the output clock signal has a clock frequency half that of the input clock signal.

10. The PLD of Claim 9, wherein the output clock signal has a rising edge corresponding to a rising edge of the input clock signal.

11. The PLD of Claim 9, wherein the output clock signal has a rising edge corresponding to a falling edge of the input clock signal.

12. The PLD of Claim 6, wherein the output clock signal has a clock frequency twice that of the input clock signal.

13. The PLD of Claim 6, wherein the output clock signal has a clock frequency N times that of the input clock signal, where N is an even number greater than two.